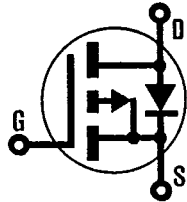


HEXFET® TRANSISTORS IRF9530



P-Channel

IRF9531

IRF9532

IRF9533

-100 Volt, 0.3 Ohm HEXFET TO-220AB Plastic Package

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The P-Channel HEXFETs are designed for applications which require the convenience of reverse polarity operation. They retain all of the features of the more common N-Channel HEXFETs such as voltage control, very fast switching, ease of paralleling, and excellent temperature stability. The P-Channel IRF9530 device is an approximate electrical complement to the N-Channel IRF520 HEXFET.

P-Channel HEXFETs are intended for use in power stages where complementary symmetry with N-Channel devices offers circuit simplification. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuit and pulse amplifiers.

Features:

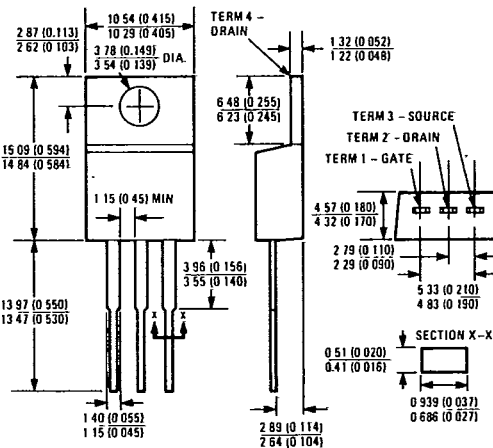
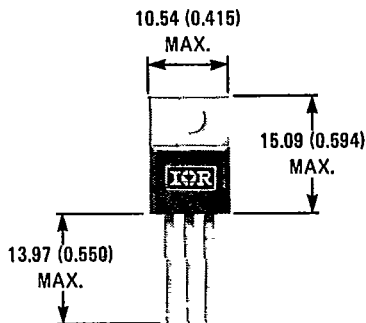
- P-Channel Versatility
- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- Excellent Temperature Stability

Product Summary

Part Number	V _{DS}	R _{DS(on)}	I _D
IRF9530	-100V	0.30Ω	-12A
IRF9531	-60V	0.30Ω	-12A
IRF9532	-100V	0.40Ω	-10A
IRF9533	-60V	0.40Ω	-10A



CASE STYLE AND DIMENSIONS



Case Style TO-220AB
Dimensions in Millimeters and (Inches)

IRF9530, IRF9531, IRF9532, IRF9533 Devices

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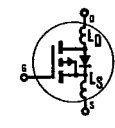
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Absolute Maximum Ratings

Parameter	IRF9530	IRF9531	IRF9532	IRF9533	Units
V _{DS} Drain - Source Voltage ①	-100	-60	-100	-60	V
V _{DGR} Drain - Gate Voltage (R _{GS} = 20 kΩ) ①	-100	-60	-100	-60	V
I _D @ T _C = 25°C Continuous Drain Current	-12	-12	-10	-10	A
I _D @ T _C = 100°C Continuous Drain Current	-7.5	-7.5	-6.5	-6.5	A
I _{DM} Pulsed Drain Current ③	-48	-48	-40	-40	A
V _{GS} Gate - Source Voltage	± 20				V
P _D @ T _C = 25°C Max. Power Dissipation	75		(See Fig. 14)		W
Linear Derating Factor	0.6		(See Fig. 14)		W/K④
I _{LM} Inductive Current, Clamped	(See Fig. 15 and 16) L = 100 μH		-40		A
T _J Operating Junction and Storage Temperature Range	-55 to 150				°C
T _{stg} Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS} Drain - Source Breakdown Voltage	IRF9530 IRF9532 IRF9531 IRF9533	-100 -60	— —	— —	V	V _{GS} = 0V I _D = -250 μA
V _{GS(th)} Gate Threshold Voltage	ALL	-2.0	—	-4.0	V	V _{DS} = V _{GS} , I _D = -250 μA
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	-500	nA	V _{GS} = -20V
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	500	nA	V _{GS} = 20V
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	-250 -1000	μA	V _{DS} = Max. Rating, V _{GS} = 0V V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C
I _{D(on)} On-State Drain Current ②	IRF9530 IRF9531 IRF9532 IRF9533	-12 -10	— —	— —	A	V _{DS} > I _{D(on)} x R _{DS(on)} max., V _{GS} = -10V
R _{DS(on)} Static Drain-Source On-State Resistance ②	IRF9530 IRF9531 IRF9532 IRF9533	— —	0.25 0.30	0.30 0.40	Ω	V _{GS} = -10V, I _D = -6.5A
g _{fs} Forward Transconductance ②	ALL	2.0	3.8	—	S (Ω)	V _{DS} > I _{D(on)} x R _{DS(on)} max., I _D = -6.5A
C _{iss} Input Capacitance	ALL	—	500	700	pF	V _{GS} = 0V, V _{DS} = -25V, f = 1.0 MHz See Fig. 10
C _{oss} Output Capacitance	ALL	—	300	450	pF	
C _{rss} Reverse Transfer Capacitance	ALL	—	100	200	pF	
t _{d(on)} Turn-On Delay Time	ALL	—	30	60	ns	V _{DD} = 0.5 BV _{DSS} , I _D = -6.5A, Z ₀ = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t _r Rise Time	ALL	—	70	140	ns	
t _{d(off)} Turn-Off Delay Time	ALL	—	70	140	ns	
t _f Fall Time	ALL	—	70	140	ns	
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	25	45	nC	
Q _{gs} Gate-Source Charge	ALL	—	13	—	nC	V _{GS} = -15V, I _D = -15A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	12	—	nC	
L _D Internal Drain Inductance	ALL	—	3.5 4.5	—	nH	
L _S Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.



Thermal Resistance

R _{thJC} Junction-to-Case	ALL	—	—	1.67	K/W④	
R _{thCS} Case-to-Sink	ALL	—	—	1.0	K/W④	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	—	—	80	K/W④	Typical socket mount

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF9530	—	—	-12	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF9531	—	—	-10	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF9530	—	—	-48	A	
		IRF9531	—	—	-40	A	
V_{SD}	Diode Forward Voltage ②	IRF9530	—	—	-6.3	V	$T_C = 25^\circ\text{C}, I_S = -12\text{A}, V_{GS} = 0\text{V}$
		IRF9531	—	—	-6.0	V	$T_C = 25^\circ\text{C}, I_S = -10\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	ALL	—	300	—	ns	$T_J = 150^\circ\text{C}, I_F = -12\text{A}, di_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovered Charge	ALL	—	1.8	—	μC	$T_J = 150^\circ\text{C}, I_F = -12\text{A}, di_F/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



- ① $T_J = 25^\circ\text{C}$ to 150°C .
- ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
- ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
- ④ $\text{K/W} = \text{K/W}$
 $\text{W/K} = \text{W/K}$

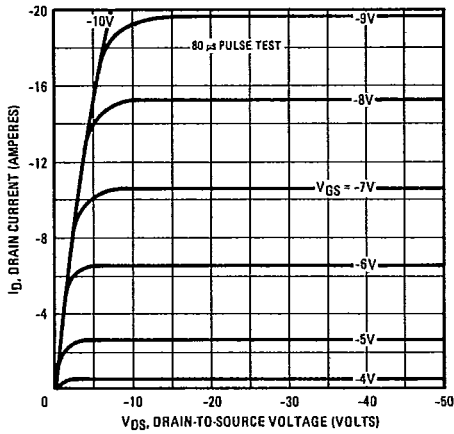


Fig. 1 – Typical Output Characteristics

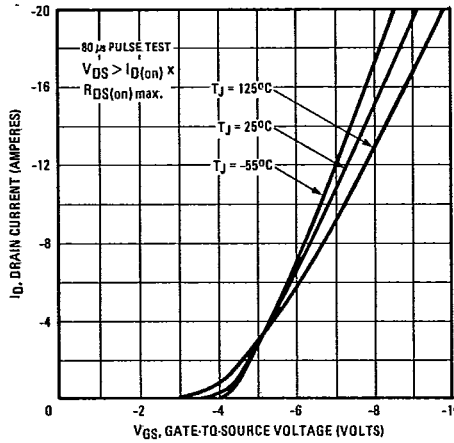


Fig. 2 – Typical Transfer Characteristics

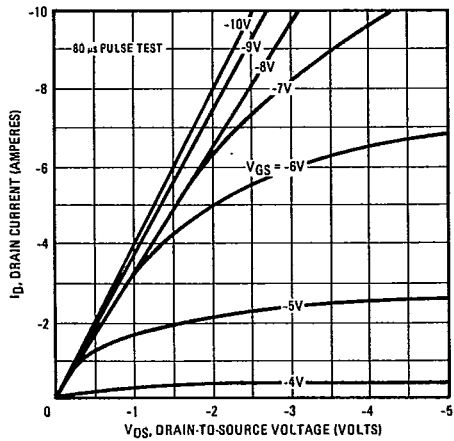


Fig. 3 – Typical Saturation Characteristics

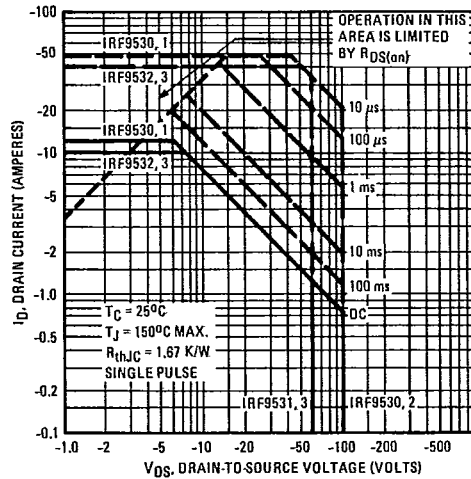


Fig. 4 – Maximum Safe Operating Area

IRF9530, IRF9531, IRF9532, IRF9533 Device
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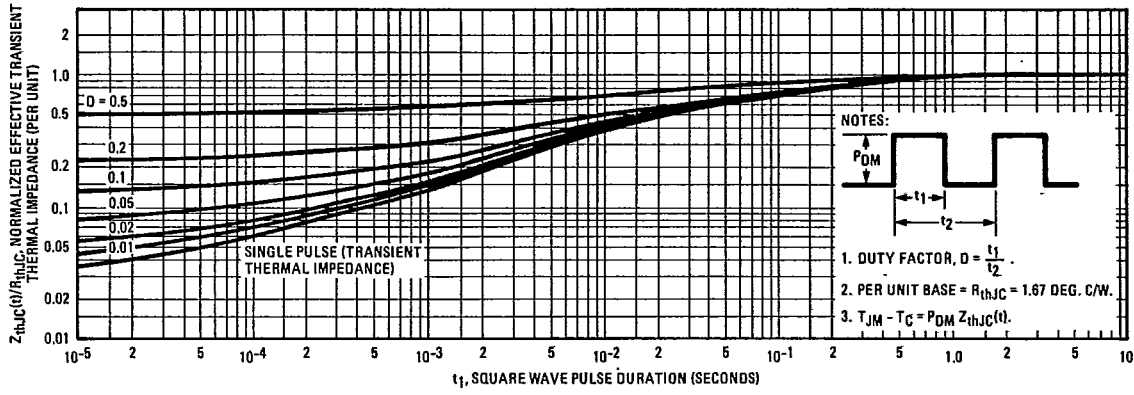


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

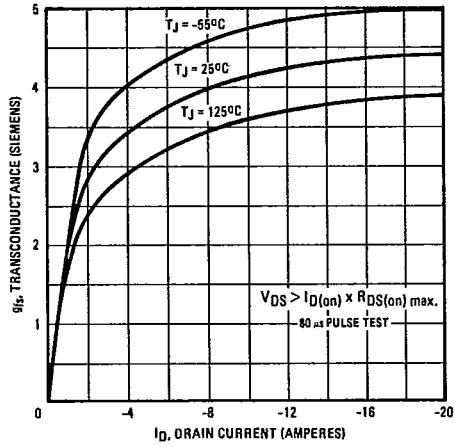


Fig. 6 – Typical Transconductance Vs. Drain Current

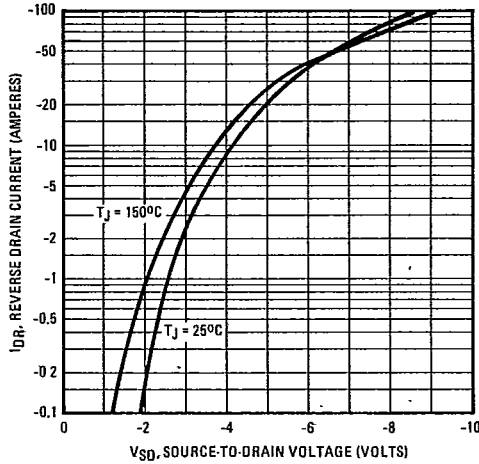


Fig. 7 – Typical Source-Drain Diode Forward Voltage

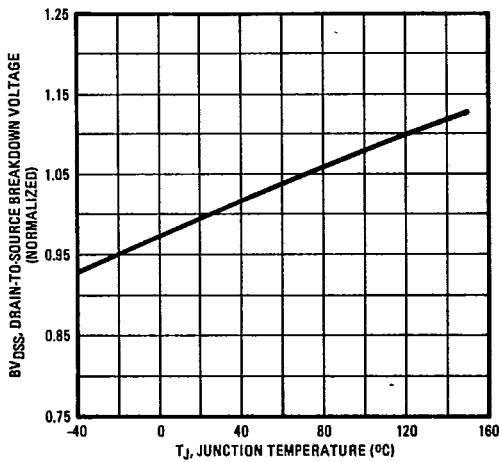


Fig. 8 – Breakdown Voltage Vs. Temperature

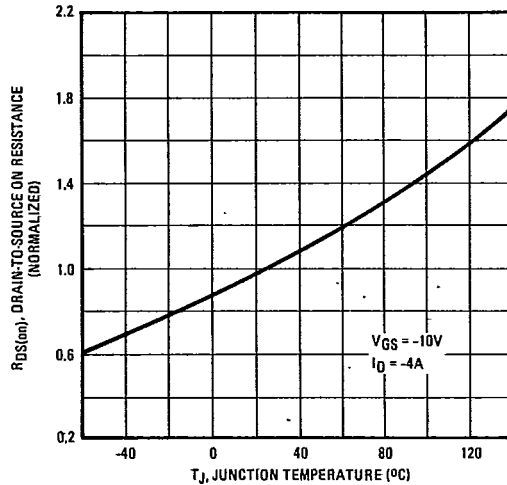


Fig. 9 – Normalized On-Resistance Vs. Temperature

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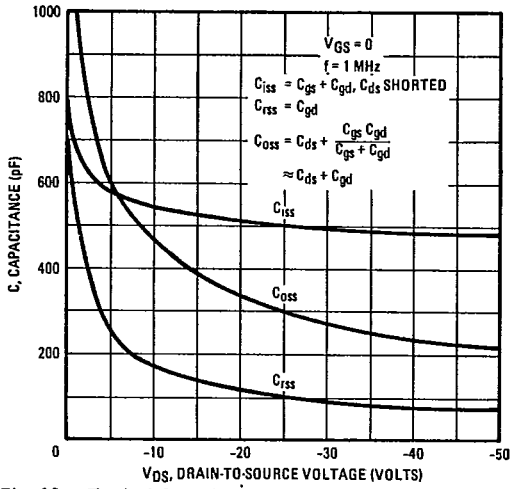


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

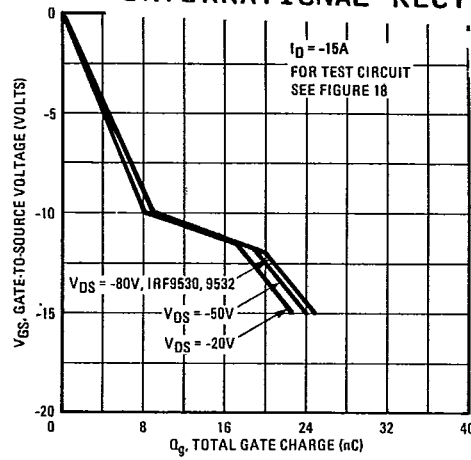


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

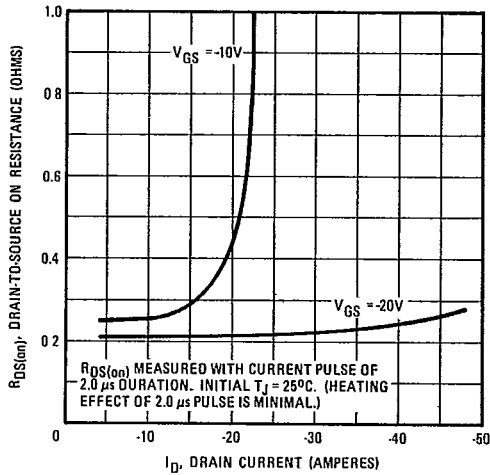


Fig. 12 - Typical On-Resistance Vs. Drain Current

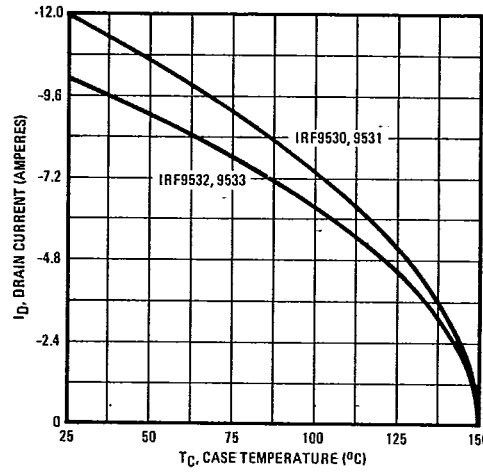


Fig. 13 - Maximum Drain Current Vs. Case Temperature

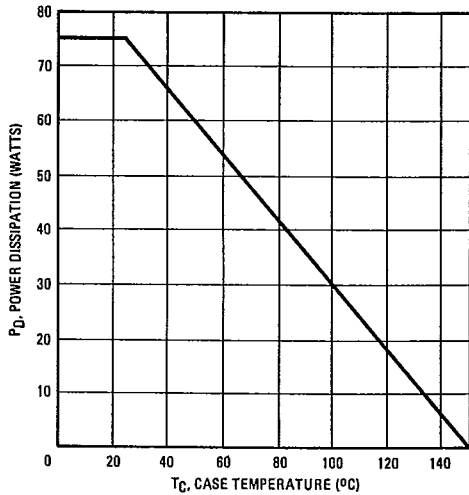


Fig. 14 - Power Vs. Temperature Derating Curve

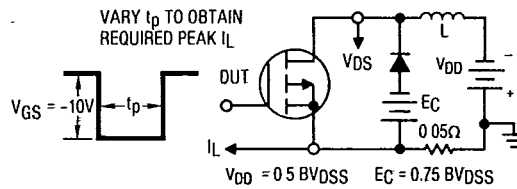


Fig. 15 - Clamped Inductive Test Circuit

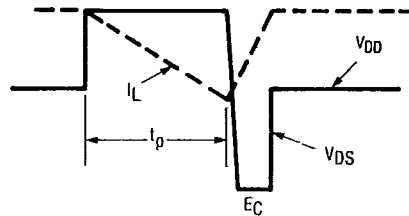


Fig. 16 - Clamped Inductive Waveforms

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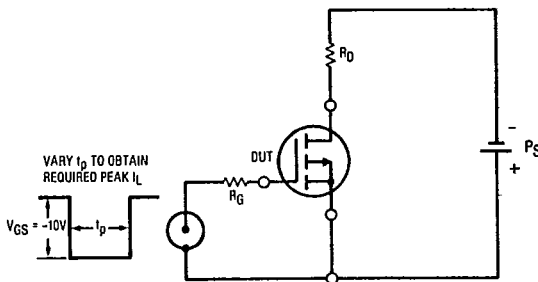


Fig. 17 - Switching Time Test Circuit

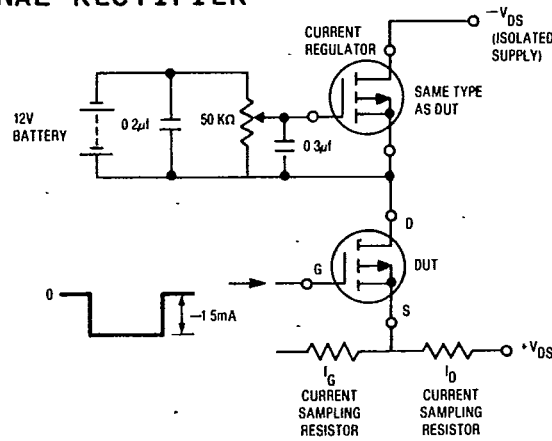
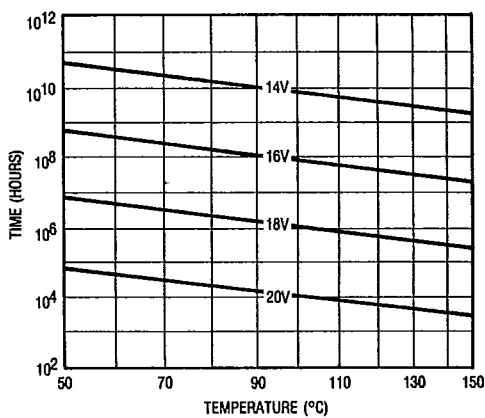
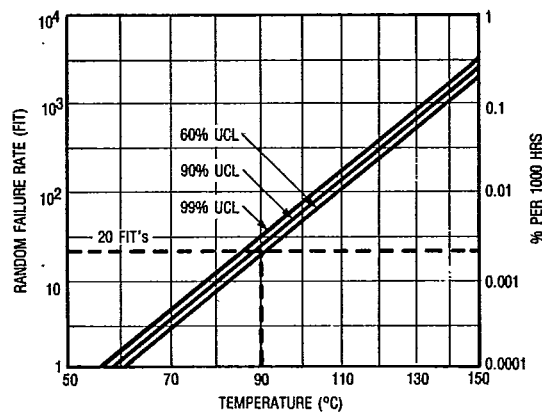


Fig. 18 - Gate Charge Test Circuit



*Fig. 19 - Typical Time to Accumulated 1% Failure



*Fig. 20 - Typical High Temperature Reverse Bias (HTRB) Failure Rate

*The data shown is correct as of April 15, 1987. This information is updated on a quarterly basis; for the latest reliability data, please contact your local IR field office.

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